I claim:

1. A system comprising:
a processor; and
a memory device coupled to the processor, the memory device including:
a main memory; and
a cache memory coupled to the processor and to the main memory to increase effective access speed between the processor and the memory device.

2. The system of claim 1, wherein:
the cache memory and main memory are on a same integrated circuit.

3. The system of claim 1, wherein:
the main memory is a flash memory.

4. The system of claim 1, wherein:
the cache memory can hold no more than sixteen addresses at the same time.

5. The system of claim 1, wherein:
the cache memory, main memory, and processor are on a same integrated circuit.

6. An apparatus comprising:

a memory device to couple to a processor through a bus, the memory device including:

a main memory; and

a cache memory coupled to the main memory to increase effective access speed between the processor and the memory device.

7. The apparatus of claim 6, wherein:

the cache memory is on a same integrated circuit as the main memory.

8. The apparatus of claim 6, wherein:

the main memory is a flash memory.

9. The apparatus of claim 6, wherein:

the cache memory can hold no more than sixteen addresses at one time.

10. A method, comprising:

requesting data from an address of a main memory;

determining if the address is contained in a cache memory located on a same integrated circuit with the main memory;

retrieving the data from the cache memory if the address is contained in the cache memory;

retrieving the data from the main memory if the address is not contained in the cache memory; and

providing the retrieved data to a requester.

11. The method of claim 10, further comprising:
if determining determines that the address is not contained in the cache memory, placing the data and the address into the cache memory.

12. The method of claim 10, wherein:
retrieving the data from main memory includes retrieving a quadword containing the data.

13. The method of claim 10, wherein:
retrieving the data from cache memory includes retrieving a quadword containing the data.

14. The method of claim 10, wherein:
the cache memory includes no more than sixteen locations for storing data.

15. The method of claim 10, wherein:
requesting data from a main memory includes requesting data from a flash memory.

16. A method, comprising:
requesting data from a plurality of sequential addresses of a main memory in a burst transfer;
determining if the addresses are contained in a cache memory located on a same integrated circuit with the main memory;

if the addresses are contained in the cache memory, retrieving the data from the cache memory;

if the addresses are not contained in the cache memory, retrieving the data from the main memory, and placing the data and at least one of the addresses into the cache memory;

initiating a transfer of the requested data to a requester;

interrupting the transfer after transferring a first portion of the requested data; and

resuming the transfer by retrieving a second portion of the requested data from the cache memory and transferring the second portion to the requester.

17. The method of claim 16, wherein:

retrieving the data from main memory includes retrieving a quadword containing the data.

18. The method of claim 16, wherein:

retrieving the data from cache memory includes retrieving a quadword containing the data.

19. The method of claim 16, wherein:

requesting data from a main memory includes requesting data from a flash memory.

20. The method of claim 16, wherein:

the cache memory includes no more than sixteen locations for storing data.